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A NEW BILATERAL FAST LINEAR GATE CIRCUIT

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A linear gate suited to transmit 2 ns minimum width pulses, is described. The minimum gate duration is 5 ns, the a.c. rejection (output for non-gated pulses) is less than 0.5 V at maximum negative amplitude corresponding to a 9 V output pulse. Rejection ratio is then 25 dB; d.c. pedestal (output for gating pulses) is 0.05 V. Attenuation of allowed pulses through the gate is 0.7 dB. A gating pulse generator is also described capable of repetition rates of 100 Mc/s.

1. Introduction

The described gate (fig. 1) can be used linearly with pulses 2 ns wide up to 9 V negative amplitude, with minimum gating width of 5 ns, at repetition rate of 100 Mc/s.

The circuit utilizes some nanosecond current steering technique applied to a balanced diode bridge, to be open to transmit pulses through the output linearily. Current steering is performed by a balanced common emitter pair of fast transistors[1]) operated in a non saturating mode. The diode bridge is realized on the same silicon wafer with planar techniques. They are now commercially available with diode controlled characteristic within 10% [2]).

During the last few years many efforts have been done about sampling balanced diode bridge[3]). Here the gating pulses are wider than the allowed ones. Diode bridge technique has given us the opportunity to utilize for a fast linear gate the pulse bilaterality with the very good transmission linearity of the diode compounds now commercially available.

The hybrid tunnel diode common base transistor coupling technique has been used[4]) in a gating pulse shaper, with profit. The circuit has few components and allows minimum gating pulse width in the nanosecond range. Repetition rate of formed pulses is over 100 MHz.

2. Gating pulse shaper

The circuit consist of a 1N3129 tunnel diode loaded with the input impedance of a common base transistor in such a way to remain in a bistable condition.

A common-base transistor acts as an unilateral buffer at the output of the diode[4–6]).

TABLE 1 Characteristics

Gated pulses circuit:	
Input pulses:	
Polarity	positive and negative
Amplitude	positive: 0 ÷ 5 V; negative: 0 ÷ 5 V
Impedance	125 ohm
Maximum pulse width	~ 3 ns less than formed gating pulse width
Minimum pulse width	~ 2 ns
Output pulses:	
Polarity	positive and negative
Impedance	= 125 ohm
Attenuation (with gating pulse)	≅ 0.7 dB
Attenuation (without gating pulse	= 25 dB (at max. amplitude)
Rejection ratio	> 20
Absolute a.c. rejection (pic to pic)	< 0.5 V(at max. amplitude)
D.c. pedestal	< 0.05 V

Gating pulse shaper:	
Input pulses:	
Trigger polarity	negative
Amplitude	4–40 mA
Impedance	50 ohm
Maximum pulse width	less than the delay of the forming cable
Minimum pulse width	1 ns
Output pulses:	
Polarity	negative
Amplitude	16 mA (for min. overdrive)
Width (variable with cable length from 5 ns minimum)	10, 20 ns
Rise and fall time (10–90%)	3 ns (measured on 330 ohm)
Cable characteristics	RG 174/21-598 50 ohm (5.2ns/m delay) or microstrip of the same characteristics

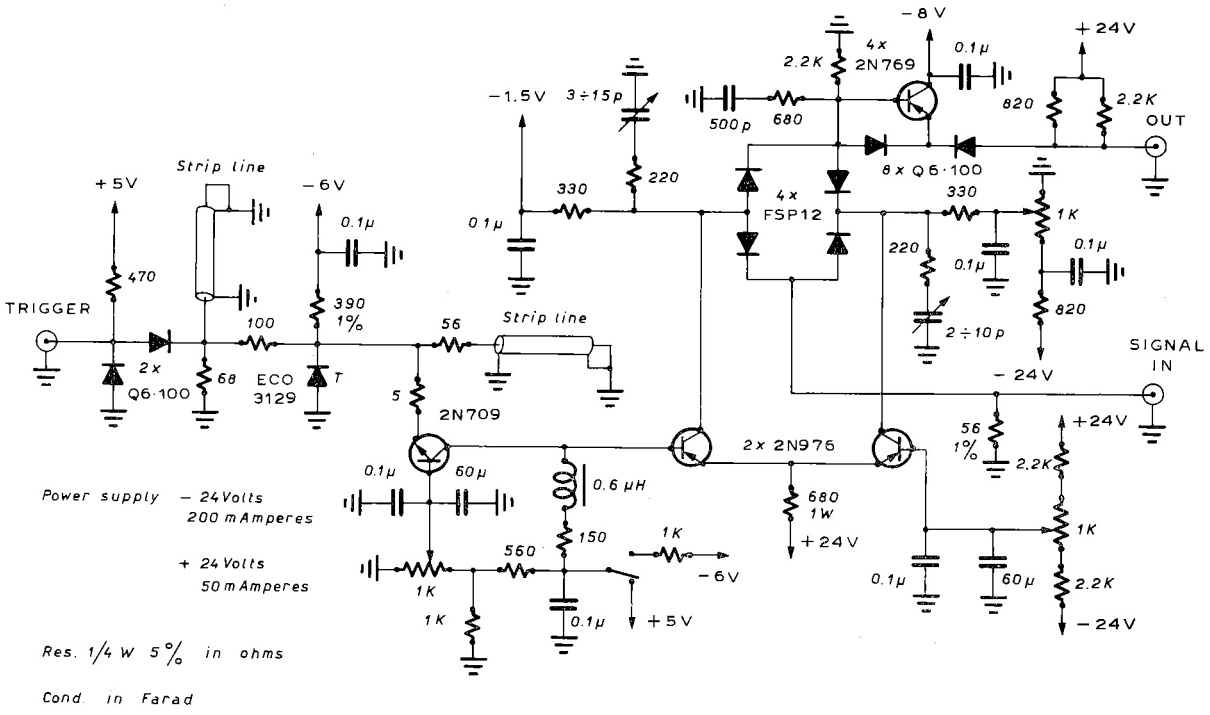

Fig. 1. Linear gate.

The diode is statically biased in its low-voltage region with 18 mA. The input pulse brings the diode into its high-voltage region; a current of about 15 mA is fed into the load transistor and remains in this region till the reset pulse is reflected from the shorted end of the cable. Fig. 2 shows the switching path in the V-1 plane of the diode.

With one meter of RG 174/U cable the pulse is

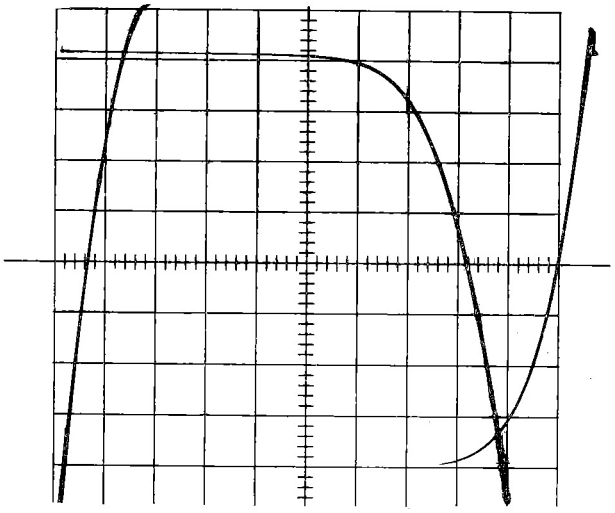

Fig. 2. Tunnel-transistor polarization of the gating pulse shaper.

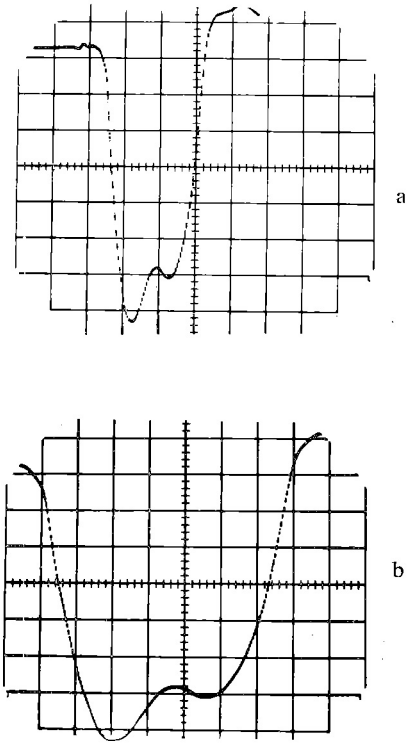

Fig. 3. Output current pulse of the gating pulse shaper (on 180 Ω load). a: 10 ns/div; 0.2 V/div. b: 2 ns/div; 0.2 V/div.

12 ns wide (fig. 3); transistor time transfer is about 0.8 ns; deadtime is less than 10 ns[7]).

3. Current switching with the long-tail pair

The circuit is formed by two 2N976 transistors mounted in a balanced common emitter pair. The circuit, as known, has very good current switching properties. In fact currents must change between transistors contemporarily and in the same amount. The total switching time (~ 2 ns) is firstly determined by the cut-off frequency of transistors common collector connection.

The first transistor is off and receives the switching signal from the output of the gating pulse shaper.

The output on the collectors are two pulses of opposite polarities and equal amplitude (~ 4 V). Their delay depends only on the delay-time difference between the two transistors: the difference in the shape depends only on the complex loads difference at the collectors (fig. 4). We have measured a maximum delay of 0.8 ns.

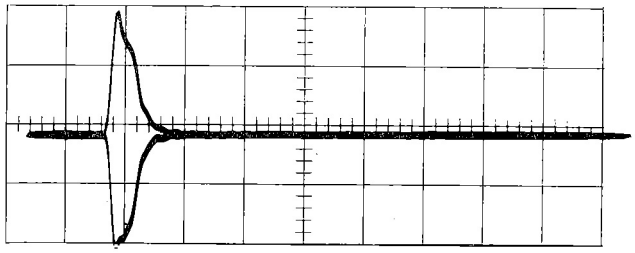

Fig. 4. Gating pulses at the long tail pair output (50 ns/cm; 2 V/cm).

4. Gate circuit and matching of the gated pulses

A fast silicon junction four diode bridge diffused on the same slide form the circuit (fig. 5).

The pulses from the long-tail-pair activate the branches ACB-ADB of the bridge, statically biased on the reverse region with 1.5 V. The pulses to be fed through the bridge are applied to point D and picked up from point C. This is a simple way to gate pulses of opposite polarities in a perfect bilateral manner.

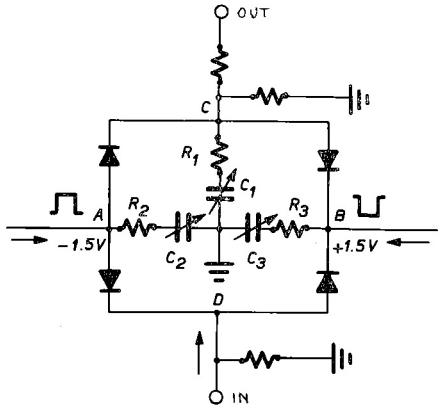

Fig. 5. Diode bridge a.c. compensation.

In the two opposite branches of the bridge will flow the same gating pulse current, if the static characteristics of the diode are identical. No d.c. pedestal will be present in the output and, if the reactive components of the branches are also identical, no a.c. pedestal will also be present (see fig. 6 for d.c. considerations)[8]).

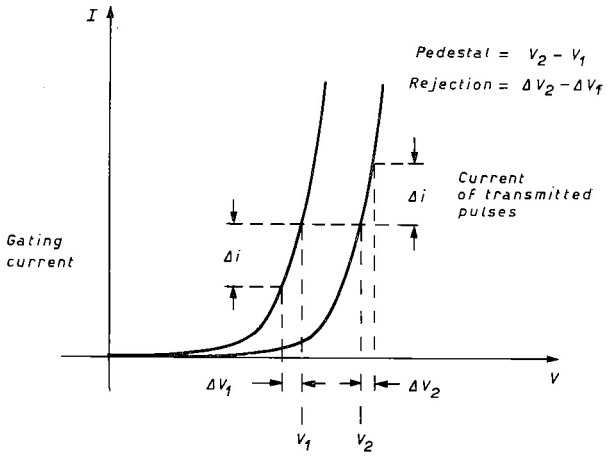

Fig. 6. Matching of two diodes of the gate.

Some amplitude difference of the gating pulses originates d.c. pedestal in the output; difference in shape or different delays give rise to an a.c. pedestal.

The reactive components in the branches which give rise to the output pedestals are mainly due to the reverse region capacitance of the diodes. 1.5 V reverse bias on the diodes assure little capacitance and low voltage excursion in the current switching circuit, at the same time.

With a reference to the pulses to be fed through the bridge, we must also consider the dynamic reactance of the diodes. Difference between branches produces attenuation dependent on shape and width of the transmitted pulses and maximum transfer current limitation. It is possible to compensate for little reactive differences in the branches with RC parallel networks (fig. 5). The compensation can be effective only in a limited range of frequencies, that means, only for some gating and gated pulse widths. Experimentally we could find very good adjustments. We have obtained 40 mV d.c. pedestal, rejection ratio better than 25 (a.c. with maximum dynamics, fig. 7 and fig. 9). The attenuation for gated pulses is less than 0.7 dB (fig. 8).

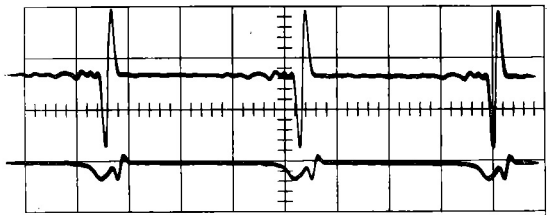

Fig. 7. Rejection ratio (1) at max. output and pedestal (2) of the gate. (50 ns/div; 0.1 V/div).

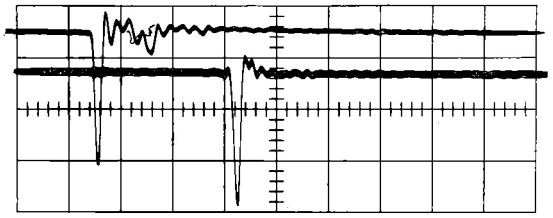

Fig. 8. Input and output of the gate. (50 ns/div; 2 V/div.).

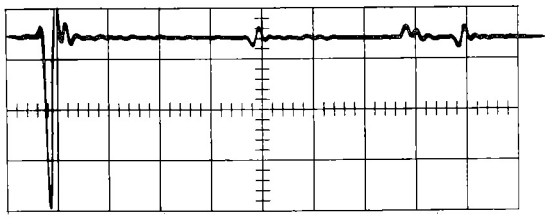

Fig. 9. Complete picture of the gate performance. (50 ns/div; 2 V/div).

Further improvements in the rejection ratio and pedestal can be achieved at a cost of larger attenuation. The linearity of the transfer through the gate is shown in fig. 10. It has been obtained gating the pulses of a standard amplitude pulse generator, through a multichannel analyzer. Standard input pulses have been previously checked in the analyzer channels that we have taken as reference.

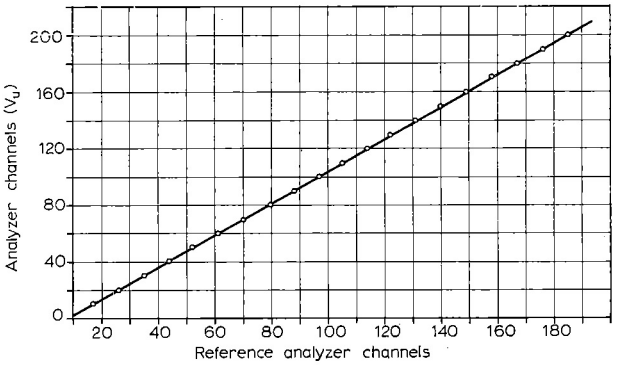

Fig. 10. Linearity of gate transfer.

Matching of input and output pulses of the bridge can be achieved with two buffer circuits.

Good matching can be provided, avoiding circuit complexity, for gated and non gated pulses, with an output emitter-follower. This can provide a high input impedance so that the input pulses can be separated quite completely from the output. Large dynamics are assured with little currents variations in the diodes.

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